

What is claimed is:

1. A process of manufacturing a semiconductor device comprising the step of chemical mechanical polishing for flattening an interlayer insulating film deposited on a wafer on which desired elements are in advance formed, wherein a stopper layer is formed on a region which will be excessively polished through the chemical mechanical polishing before or after forming the interlayer insulating film.
- 10 2. A process according to claim 1, wherein the stopper layer has a thickness greater than an intended thickness of the interlayer insulating film to be obtained after the polishing by a thickness of the interlayer insulating film reduced by the polishing.
- 15 3. A process according to claim 1 further comprising the step of photolithography for forming a connection hole in the interlayer insulating film, wherein the stopper layer has a width greater than that of a resist layer to be removed from a wafer periphery portion in the photolithography step.
- 20 4. A process according to claim 1, wherein the stopper layer is a silicon nitride film.

5. A process according to claim 1, wherein the interlayer insulating film is a silicon oxide film.

6. A process according to claim 3, wherein the width of
5 the resist layer to be removed from the wafer periphery portion
is 3-4 mm.

7. A process according to claim 1, wherein the stopper
layer is removed after the chemical mechanical polishing.

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8. A process according to claim 2, wherein the stopper
layer has a thickness greater than the intended thickness of
the interlayer insulating film by 50-700 Å .